WHAT IS CLAIMED IS:

1. An electrical circuit, comprising:

a differential amplifier, comprising:

an input circuit in communication with a differential input of the differential amplifier, the input circuit comprising:

a first input transistor; and

a second input transistor,

wherein base electrodes of the first and second input transistors are in communication with the differential input, and

wherein emitter electrodes of the first and second input transistors are in communication with each other and a first current source;

a start-up circuit in communication with the input circuit,

wherein the start-up circuit is configured to generate a start-up signal to enable subsequent operation of the differential amplifier, the start-up circuit comprising:

a first start-up transistor; and

a second start-up transistor,

wherein base electrodes of the first and second start-up transistors are in communication with a bias input,

wherein emitter electrodes of the first and second start-up transistors are in communication with each other and with the first current source, and

wherein collector electrodes of the first and second start-up transistors are in communication with collector electrodes of the first and second input transistors, respectively; and

an output circuit in communication with the input circuit and the start-up circuit,

wherein the output circuit is in communication with a differential output of the differential amplifier, the output circuit comprising:

a first output transistor;

a second output transistor;

a first impedance circuit; and

a second impedance circuit,

wherein base electrodes of the first and second output transistors are in communication with the first and second impedance circuits, respectively, and the collector electrodes of the first and second input transistors, respectively,

wherein emitter electrodes of the first and second output transistors are in communication with each other and with the first current source, and

wherein collector electrodes of the first and second output transistors are in communication with the first and second impedance circuits, respectively, and the differential output.

2. The electrical circuit of claim 1, wherein the first and second impedance circuits each comprise a capacitor and a resistor in series,

3. The electrical circuit of claim 1, wherein the differential amplifier further comprises:

a common-mode feedback circuit in communication with the differential output and second and third current sources,

wherein the second and third current sources are in communication with the input and start-up circuits.

4. The electrical circuit of claim 3, wherein the common-mode feedback circuit comprises:

a comparator for comparing a feedback signal from the differential output with a predetermined reference signal to generate a comparison signal,

wherein the comparison signal controls the second and third current sources to control an output level of the differential amplifier; and

first and second resistors in communication with the differential output and an input of the comparator.

5. The electrical circuit of claim 3, wherein the differential amplifier further comprises:

fourth and fifth current sources in communication with the input and start-up circuits; and

sixth and seventh current sources in communication with the differential output and the output circuit.

6. The electrical circuit of claim 1, wherein the start-up circuit ceases generation of the start-up signal when the operation of the differential amplifier reaches a steady-state.

7. The electrical circuit of claim 1, wherein the differential amplifier comprises a fully differential operational amplifier.

8. The electrical circuit of claim 1, wherein the differential amplifier comprises a Gm cell.

9. The electrical circuit of claim 1, wherein the electrical circuit is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

10. An electrical circuit, comprising:

a differential amplifier means, comprising:

an input circuit means for receiving a differential input signal,

wherein the input circuit means is in communication with a differential input means of the differential amplifier means, and

wherein the input circuit means comprises:

first and second input amplifier means,

wherein each of the first and second input amplifier means includes first, second and third electrode means,

wherein the first electrode means of the first and second input amplifier means are in communication with the differential input means, and

wherein the second electrode means of the first and second input amplifier means are in communication with each other and a first current source means;

a start-up circuit means for generating a start-up signal to enable subsequent operation of the differential amplifier means,

wherein the start-up circuit means is in communication with the input circuit means, and

wherein the start-up circuit comprises:

first and second start-up amplifier means,

wherein each of the first and second start-up amplifier means includes first, second and third electrode means,

wherein the first electrode means of the first and second start-up amplifier means are in communication with a bias input means,

wherein the second electrode means of the first and second start-up amplifier means are in communication with each other and with the first current source means, and

wherein the third electrode means of the first and second start-up amplifier means are in communication with the third electrode means of the first and second input amplifier means, respectively; and

an output circuit means for outputting a differential output signal,

wherein the output circuit means is in communication with a differential output means of the differential amplifier means and in communication with the input circuit means and the start-up circuit means, and

wherein the output circuit comprises:

first and second output amplifier means,

wherein each of the first and second output amplifier means includes first, second and third electrode means; and

first and second impedance means,

wherein the first electrode means of the first and second output amplifier means are in communication with the first and second impedance means, respectively, and the third electrode means of the first and second input amplifier means, respectively,

wherein the second electrode means of the first and second output amplifier means are in communication with each other and with the first current source means, and

wherein the third electrode means of the first and second output amplifier means are in communication with the first and second impedance means, respectively, and the differential output means.

11. The electrical circuit of claim 10, wherein the differential amplifier means further comprises:

feedback means in communication with the differential output means and second and third current source means,

wherein the second and third current source means are in communication with the input and start-up circuit means.

12. The electrical circuit of claim 11, wherein the feedback means comprises:

means for comparing a feedback signal from the differential output means with a predetermined reference signal to generate a comparison signal,

wherein the comparison signal controls the second and third current source means to control an output level of the differential amplifier means; and

first and second resistive means in communication with the differential output means and an input of the comparator means.

13. The electrical circuit of claim 11, wherein the differential amplifier means further comprises:

fourth and fifth current source means in communication with the input and start-up means; and

sixth and seventh current source means in communication with the differential output means and the output circuit means.

14. The electrical circuit of claim 10, wherein the start-up circuit means ceases generation of the start-up signal when the operation of the differential amplifier means reaches a steady-state.

15. The electrical circuit of claim 10, wherein the electrical circuit is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

16. An electrical circuit, comprising:

an amplifier, comprising:

an input circuit in communication with an input of the amplifier;

a start-up circuit in communication with the input circuit,

wherein the start-up circuit is configured to generate a start-up signal to enable subsequent operation of the amplifier; and

an output circuit in communication with an output of the amplifier and in communication with the input circuit and the start-up circuit.

17. The electrical circuit of claim 16, wherein the amplifier comprises a differential amplifier,

wherein the input of the amplifier comprises a differential input, and

wherein the output of the amplifier comprises a differential output.

18. The electrical circuit of claim 16, wherein the input circuit comprises:

a first input transistor; and

a second input transistor,

wherein base electrodes of the first and second input transistors are in communication with the input, and

wherein emitter electrodes of the first and second input transistors are in communication with each other and a first current source.

19. The electrical circuit of claim 16, wherein the start-up circuit comprises:

a first start-up transistor; and

a second start-up transistor,

wherein base electrodes of the first and second start-up transistors are in communication with a bias input,

wherein emitter electrodes of the first and second start-up transistors are in communication with each other and with a first current source, and

wherein collector electrodes of the first and second start-up transistors are in communication with collector electrodes of first and second input transistors, respectively.

20. The electrical circuit of claim 16, wherein the output circuit comprises:

a first output transistor;

a second output transistor;

a first impedance circuit; and

a second impedance circuit,

wherein base electrodes of the first and second output transistors are in communication with the first and second impedance circuits, respectively, and collector electrodes of first and second input transistors, respectively,

wherein emitter electrodes of the first and second output transistors are in communication with each other and with a first current source,

wherein collector electrodes of the first and second output transistors are in communication with the first and second impedance circuits, respectively, and the output.

21. The electrical circuit of claim 20, wherein each of the first and second impedance circuits comprises a capacitor and a resistor in series.

22. The electrical circuit of claim 16, wherein the amplifier further comprises:

a common-mode feedback circuit in communication with the output and second and third current sources,

wherein the second and third current sources are in communication with the input and start-up circuits.

23. The electrical circuit of claim 22, wherein the common-mode feedback circuit comprises:

a comparator for comparing a feedback signal from the output with a predetermined reference signal to generate a comparison signal,

wherein the comparison signal controls the second and third current sources to control an output level of the amplifier; and

first and second resistors in communication with the output and an input of the comparator.

24. The electrical circuit of claim 22, wherein the amplifier further comprises:

fourth and fifth current sources in communication with the input and start-up circuits; and

sixth and seventh current sources in communication with the output and the output circuit.

25. The electrical circuit of claim 16, wherein the start-up circuit ceases generation of the start-up signal when the operation of the amplifier reaches a steady-state.

26. The electrical circuit of claim 17, wherein the amplifier comprises a fully differential operational amplifier.

27. The electrical circuit of claim 17, wherein the amplifier comprises a Gm cell.

28. The electrical circuit of claim 16, wherein the electrical circuit is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

29. An electrical circuit, comprising:

an amplifier means, comprising:

an input circuit means for receiving an input signal,

wherein the input circuit means is in communication with an input means of the amplifier means;

a start-up circuit means for generating a start-up signal to enable subsequent operation of the amplifier means,

wherein the start-up circuit means is in communication with the input circuit means; and

an output circuit means for outputting an output signal,

wherein the output circuit means is in communication with an output means of the amplifier means and in communication with the input circuit means and the start-up circuit means.

30. The electrical circuit of claim 29, wherein the amplifier means comprises a differential amplifier means,

wherein the input means of the amplifier means comprises a differential input means, and

wherein the output means of the amplifier means comprises a differential output means.

31. The electrical circuit of claim 29, wherein the input circuit means comprises:

first and second input amplifier means,

wherein each of the first and second input amplifier means includes first, second and third electrode means,

wherein the first electrode means of the first and second input amplifier means are in communication with the input means, and

wherein the second electrode means of the first and second input amplifier means are in communication with each other and a first current source means.

32. The electrical circuit of claim 29, wherein the start-up circuit means comprises:

first and second start-up amplifier means,

wherein each of the first and second start-up amplifier means includes first, second and third electrode means,

wherein the first electrode means of the first and second start-up amplifier means are in communication with a bias input means,

wherein the second electrode means of the first and second start-up amplifier means are in communication with each other and with a first current source means, and

wherein the third electrode means of the first and second start-up amplifier means are in communication with third electrode means of first and second input amplifier means, respectively.

33. The electrical circuit of claim 29, wherein the output circuit means comprises:

first and second output amplifier means,

wherein each of the first and second output amplifier means includes first, second and third electrode means; and

first and second impedance means,

wherein the first electrode means of the first and second output amplifier means are in communication with the first and second impedance means, respectively, and third electrode means of first and second input amplifier means, respectively,

wherein the second electrode means of the first and second output amplifier means are in communication with each other and with a first current source means, and

wherein the third electrode means of the first and second output amplifier means are in communication with the first and second impedance means, respectively, and the output means.

34. The electrical circuit of claim 29, wherein the amplifier means further comprises:

feedback means in communication with the output means and second and third current source means,

wherein the second and third current source means are in communication with the input and start-up circuit means.

35. The electrical circuit of claim 34, wherein the feedback means comprises:

means for comparing a feedback signal from the output means with a predetermined reference signal to generate a comparison signal,

wherein the comparison signal controls the second and third current source means to control an output level of the amplifier means; and

first and second resistive means in communication with the output means and an input of the comparator means.

36. The electrical circuit of claim 34, wherein the amplifier means further comprises:

fourth and fifth current source means in communication with the input and start-up circuit means; and

sixth and seventh current source means in communication with the output means and the output circuit means.

37. The electrical circuit of claim 29, wherein the start-up circuit means ceases generation of the start-up signal when the operation of the amplifier means reaches a steady-state.

38. The electrical circuit of claim 29, wherein the electrical circuit is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

39. A method of starting up an electrical circuit, comprising the steps of:

applying a first signal to a start-up circuit of an amplifier;

generating a start-up signal, using the start-up circuit, in response to the first signal to enable subsequent operation of the amplifier; and

generating an output signal at an output of the amplifier in response to the start-up signal.

40. The method of claim 39, wherein the amplifier comprises a differential amplifier,

wherein an input of the amplifier comprises a differential input, and

wherein the output of the amplifier comprises a differential output.

41. The method of claim 39, comprising the steps of:

comparing a feedback signal from the output with a predetermined reference signal to generate a comparison signal; and

controlling an output level of the output signal of the amplifier using the comparison signal.

42. The method of claim 41, comprising the steps of:

applying the output signal to an input of the amplifier; and

operating the amplifier in a steady-state mode.

43. The method of claim 42, comprising the step of:

ceasing generation of the start-up signal by the start-up circuit when the operation of the amplifier reaches the steady-state mode.

44. The method of claim 39, wherein the method is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

45. An electrical circuit, comprising:

a plurality of amplifiers, wherein each of the plurality of amplifiers comprises:

an input circuit in communication with an input of the amplifier;

a start-up circuit in communication with the input circuit,

wherein the start-up circuit is configured to generate a start-up signal to enable subsequent operation of the amplifier; and

an output circuit in communication with an output of the amplifier and in communication with the input circuit and the start-up circuit;

wherein respective inputs of a first and a second amplifier of the plurality of amplifiers are in communication with outputs of a third amplifier of the plurality of amplifiers, and

wherein outputs of the second amplifier are in communication with inputs of the third amplifier.

46. The electrical circuit of claim 45, wherein each of the plurality of amplifiers comprises a differential amplifier,

wherein the input of each of the plurality of amplifiers comprises a differential input, and

wherein the output of each of the plurality of amplifiers comprises a differential output.

47. The electrical circuit of claim 45, wherein the input circuit of each of the plurality of amplifiers comprises:

a first input transistor; and

a second input transistor,

wherein base electrodes of the first and second input transistors are in communication with the input, and

wherein emitter electrodes of the first and second input transistors are in communication with each other and a first current source.

48. The electrical circuit of claim 45, wherein the start-up circuit of each of the plurality of amplifiers comprises:

a first start-up transistor; and

a second start-up transistor,

wherein base electrodes of the first and second start-up transistors are in communication with a bias input,

wherein emitter electrodes of the first and second start-up transistors are in communication with each other and with a first current source, and

wherein collector electrodes of the first and second start-up transistors are in communication with collector electrodes of first and second input transistors, respectively.

49. The electrical circuit of claim 45, wherein the output circuit of each of the plurality of amplifiers comprises:

a first output transistor;

a second output transistor;

a first impedance circuit; and

a second impedance circuit,

wherein base electrodes of the first and second output transistors are in communication with the first and second impedance circuits, respectively, and collector electrodes of first and second input transistors, respectively,

wherein emitter electrodes of the first and second output transistors are in communication with each other and with a first current source,

wherein collector electrodes of the first and second output transistors are in communication with the first and second impedance circuits, respectively, and the output.

50. The electrical circuit of claim 49, wherein each of the first and second impedance circuits comprises a capacitor and a resistor in series.

51. The electrical circuit of claim 45, wherein each of the plurality of amplifiers further comprises:

a common-mode feedback circuit in communication with the output and second and third current sources,

wherein the second and third current sources are in communication with the input and start-up circuits.

52. The electrical circuit of claim 51, wherein the common-mode feedback circuit of each of the plurality of amplifiers comprises:

a comparator for comparing a feedback signal from the output with a predetermined reference signal to generate a comparison signal,

wherein the comparison signal controls the second and third current sources to control an output level of the amplifier; and

first and second resistors in communication with the output and an input of the comparator.

53. The electrical circuit of claim 51, wherein each of the plurality of amplifiers further comprises:

fourth and fifth current sources in communication with the input and start-up circuits; and

sixth and seventh current sources in communication with the output and the output circuit.

54. The electrical circuit of claim 45, wherein the start-up circuit of each of the plurality of amplifiers ceases generation of the respective start-up signal when the operation of the respective amplifier reaches a steady-state.

55. The electrical circuit of claim 45, wherein outputs of the first amplifier are in communication with inputs of the third amplifier,

wherein a first impedance circuit is in communication between an input and an output of each of the first and second amplifiers, and

wherein a second impedance circuit is in communication between an input and an output of the third amplifier.

56. The electrical circuit of claim 55, wherein the first impedance circuit comprises a resistor and a capacitor in parallel, and

wherein the second impedance circuit comprises a capacitor.

57. The electrical circuit of claim 46, wherein each of the plurality of amplifiers comprises a fully differential operational amplifier.

58. The electrical circuit of claim 46, wherein each of the plurality of amplifiers comprises a Gm cell.

59. The electrical circuit of claim 58, wherein outputs of the first amplifier are in communication with inputs of the first amplifier,

wherein an input of the first amplifier and an input and an output of the second amplifier are in communication with an impedance circuit, and

wherein inputs of the third amplifier are in communication with outputs of the second amplifier and outputs of the third amplifier are in communication with inputs of the first and second amplifiers.

60. The electrical circuit of claim 59, wherein the impedance circuit comprises at least one capacitor in communication with a reference voltage.

61. The electrical circuit of claim 45, wherein the electrical circuit is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

62. An electrical circuit, comprising:

a plurality of amplifier means, wherein each of the plurality of amplifier means comprises:

an input circuit means for receiving an input signal,

wherein the input circuit means is in communication with an input means of the amplifier means;

a start-up circuit means for generating a start-up signal to enable subsequent operation of the amplifier means,

wherein the start-up circuit means is in communication with the input circuit means; and

an output circuit means for outputting an output signal,

wherein the output circuit means is in communication with an output means of the amplifier means and in communication with the input circuit means and the start-up circuit means;

wherein respective input means of a first and a second amplifier means of the plurality of amplifier means are in communication with output means of a third amplifier means of the plurality of amplifier means, and

wherein output means of the second amplifier means are in communication with input means of the third amplifier means.

63. The electrical circuit of claim 62, wherein each of the plurality of amplifier means comprises a differential amplifier means,

wherein the input means of each of the plurality of amplifier means comprises a differential input means, and

wherein the output means of each of the plurality of amplifier means comprises a differential output means.

64. The electrical circuit of claim 62, wherein the input circuit means of each of the plurality of amplifier means comprises:

first and second input amplifier means,

wherein each of the first and second input amplifier means includes first, second and third electrode means,

wherein the first electrode means of the first and second input amplifier means are in communication with the input means, and

wherein the second electrode means of the first and second input amplifier means are in communication with each other and a first current source means.

65. The electrical circuit of claim 62, wherein the start-up circuit of each of the plurality of amplifier means comprises:

first and second start-up amplifier means,

wherein each of the first and second start-up amplifier means includes first, second and third electrode means,

wherein the first electrode means of the first and second start-up amplifier means are in communication with a bias input means,

wherein the second electrode means of the first and second start-up amplifier means are in communication with each other and with a first current source means, and

wherein the third electrode means of the first and second start-up amplifier means are in communication with third electrode means of first and second input amplifier means, respectively.

66. The electrical circuit of claim 62, wherein the output circuit of each of the plurality of amplifier means comprises:

first and second output amplifier means,

wherein each of the first and second output amplifier means includes first, second and third electrode means; and

first and second impedance means,

wherein the first electrode means of the first and second output amplifier means are in communication with the first and second impedance means, respectively, and third electrode means of first and second input amplifier means, respectively,

wherein the second electrode means of the first and second output amplifier means are in communication with each other and with a first current source means, and

wherein the third electrode means of the first and second output amplifier means are in communication with the first and second impedance means, respectively, and the output means.

67. The electrical circuit of claim 62, wherein each of the plurality of amplifier means further comprises:

feedback means in communication with the output means and second and third current source means,

wherein the second and third current source means are in communication with the input and start-up circuit means.

68. The electrical circuit of claim 67, wherein the feedback means of each of the plurality of amplifier means comprises:

means for comparing a feedback signal from the output means with a predetermined reference signal to generate a comparison signal,

wherein the comparison signal controls the second and third current source means to control an output level of the amplifier means; and

first and second resistive means in communication with the output means and an input of the comparator means.

69. The electrical circuit of claim 67, wherein each of the plurality of amplifier means further comprises:

fourth and fifth current source means in communication with the input and start-up circuit means; and

sixth and seventh current source means in communication with the output means and the output circuit means.

70. The electrical circuit of claim 62, wherein the start-up circuit means of each of the plurality of amplifier means ceases generation of the respective start-up signal when the operation of the respective amplifier means reaches a steady-state.

71. The electrical circuit of claim 62, wherein output means of the first amplifier means are in communication with input means of the third amplifier means,

wherein a first impedance means is in communication between an input means and an output means of each of the first and second amplifier means, and

wherein a second impedance means is in communication between an input means and an output means of the third amplifier means.

72. The electrical circuit of claim 62, wherein output means of the first amplifier means are in communication with input means of the first amplifier means, and

wherein an input means of the first amplifier means and an input means and an output means of the second amplifier means are in communication with an impedance means, and

wherein input means of the third amplifier means are in communication with output means of the second amplifier means and output means of the third amplifier means are in communication with input means of the first and second amplifier means.

73. The electrical circuit of claim 62, wherein the electrical circuit is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.

74. A method of starting up an electrical circuit, comprising the steps of:

applying a first signal to a start-up circuit of each of a plurality of amplifiers;

generating a start-up signal in each of the plurality of amplifiers, using the respective start-up circuit, in response to each first signal to enable subsequent operation of the respective amplifier; and

generating an output signal at an output of each of the plurality of amplifiers in response to the respective start-up signal.

75. The method of claim 74, wherein each of the plurality of amplifiers comprises a differential amplifier,

wherein an input of each of the plurality of amplifiers comprises a differential input, and

wherein the output of each of the plurality of amplifiers comprises a differential output.

76. The method of claim 74, comprising the steps of:

comparing a feedback signal from the output of each of the plurality of amplifiers with a predetermined reference signal to generate a respective comparison signal; and

controlling an output level of the output signal of each of the plurality of amplifiers using the respective comparison signal.

77. The method of claim 76, comprising the steps of:

applying the output signal of one of the plurality of amplifiers to an input of another one of the plurality of amplifiers; and

operating each of the plurality of amplifiers in a steady-state mode.

78. The method of claim 77, comprising the step of:

ceasing generation of the start-up signal by the respective start-up circuit of each of the plurality of amplifiers, when the operation of the respective amplifier reaches the steady-state mode.

79. The method of claim 74, wherein the method is compliant with a standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11g and 802.11i.